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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,570	02/18/2004	Giovanni Cesura	02-CA-467/GC	9296

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EXAMINER	
WAMSLEY, PATRICK G	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,570	CESURA ET AL.	
	Examiner	Art Unit	
	Patrick G. Wamsley	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 10, 14, 21-22* is/are rejected.

7)☒ Claim(s) *7-9,11-13 and 15-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-6, 10, 14, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art, hereafter APA, in view of U.S. Patent 6,735,422 to Baldwin et al, hereafter Baldwin.

For claim 1, APA, as depicted in Figure 1, discloses an analog-to-digital converter, hereafter ADC [100], comprising at least one stage [105] for converting an analog input signal [X (z)] into a digital output signal [U (z)] using a parallel quantizer [115] comparing the analog input signal [X (z)] with a plurality of threshold values in parallel [Page 2, lines 3-4].

Unlike claim 1, APA lacks means for estimating an analog correction signal. In contrast, Baldwin provides feedback loops for an ADC [313].

Specifically, Baldwin provides a DAC [337] to compensate for DC offset, corresponding to the recited quantization error. At the time of the invention, it would have been obvious to one of ordinary skill in the art to have applied Baldwin's DC compensation teachings to APA's ADC. The motivation would have been to compensate for DC offset errors, as suggested by Baldwin, [col. 3, lines 17-22].

Independent claim 21 restates these apparatus limitations in method format. Independent claim 22 claims the same limitations in system format, adding a conventional computing circuit, clearly present in APA.

For claims 2 and 4, APA discloses a parallel quantizer [115] comprising a plurality of comparators [410] and at least one capacitor [430]. In the APA / Baldwin combination, Baldwin's compensation signal would charge APA's capacitor.

For claim 3, APA discloses a plurality of stages [105 / 110], including at least one stage [105] and at least one further stage [110], the plurality of stages [105 / 110] being cascade connected [Page 8, line 23] in a sequence, wherein each stage different from a last stage in the sequence [110] includes means [120 / 140] for determining an analog residue indicative of the corresponding quantization error and means [145] for generating the analog input signal for a next stage in the sequence according to the analog residue.

For claim 5, Baldwin's DC DAC [337] converts a digital correction signal, based upon a DC estimate signal [col. 3, lines 31-35], into an analog correction signal.

For claims 6 and 14, APA discloses that each stage [147] following the selected stage [105] has a resolution lower than the resolution of the selected stage [105].

For claim 10, APA discloses means [148] for combining the digital output signals of a plurality of stages [147] into a digital residue signal.

Allowable Subject Matter

Claims 7-9, 11-13, and 15-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the references of record neither reveal nor render obvious the recited combination including the concepts of reducing the resolution of a digital correction signal [claims 7, 11, and 17], setting the dynamic range of an analog correction signal relative to the quantization error range [claims 8, 12, 15, and 19], and using the combination of a digital filter and an integrator to calculate a digital correction signal on the basis of a digital residue [claims 9, 13, 16, 18, and 20].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 6,693,863 to Shoji et al provides an asymmetry correction circuit [6] for an ADC [7]. U.S. Patent 6,522,282 to Elbornsson estimates timing offsets in parallel ADCs. U.S. Patent 6,229,467 to Eklund et al uses histograms to correct for ADC gain and offset errors. U.S. Patent 6,124,820 to Norman discloses error correction stages for pipelined ADCs. U.S. Patent 5,812,077 to Boie describes error correction [9] for ADCs [8/10]. U.S. Patent 5,479,096 to Szczyrbak et al provides gain and offset correction for ADCs.

U.S. Patent 5,172,115 to Kerth et al corrects error offsets in an ADC. U.S. Patent 4,972,189 to Polito corrects for DC offset in ADCs. U.S. Patent 4,947,168 to Myers calibrates an ADC for offset errors [37]. U.S. Patent 3,641,563 to Cushman provides an error correction circuit for ADCs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick G. Wamsley whose telephone number is (571) 272-1814. The official facsimile number is (571) 273-8300. An alternate facsimile number, (571) 273-1814, should only be used for unofficial documents.

Patrick G. Wamsley

September 22, 2005